EXPANSION PLANE FOR PQFP/TQFP IR – PACKAGE DESIGN

ABSTRACT OF THE DISCLOSURE

Provided is a lead frame package with an expansion plane to minimize electrical parasitics introduced into the semiconductor chip's electrical system (e.g., power delivery system, signal loops, etc.). Also provided are methods for assembling such lead frame packages into various semiconductor packages. Generally, a lead frame package includes a down set die attach pad over an underlying bottom plate. Both the die attach pad and the bottom plate may be used as intermediary connections for either power or ground connections. As compared to conventional lead frame package having an intermediary connection, the lead frame packages of the present invention can provide for any combination of shorter wire bond lengths, more wire bond connections, improved power delivery system, or reduced amounts of electrical parasitics.